Notice of Allowability	Application No.	Applicant(s)	
	10/789,038	FORBES ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed August 05 and phone/fax communications on September 22 and 23, 2005*.

2. ☒ The allowed claim(s) is/are *1-6,9-11 and 14-42*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/27; 6/24; 8/20; 12/20/04; 8/5/05; 9/19/05;
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

HUAN HOANG
PRIMARY EXAMINER

DETAILED ACTION

1. Applicants' Information Disclosure Statements, IDS, filed February 27 2004, June 24 2004, August 20 2004, December 20 2004, August 05 2005, and September 19 2005 have been considered.

Election/Restrictions

2. Applicant's election without traverse of claims 1 – 17 in the reply filed on August 05, 2005 is acknowledged.

3. Claims 1 – 17 are generic and allowable. Accordingly, the restriction requirement as to the encompassed species is hereby withdrawn and claims 18 – 40, directed to the species of a floating/vertical floating gate transistor having a tunnel barrier of less than 1.5eV are no longer withdrawn from consideration since all of the claims to this species depend from or otherwise include each of the limitations of an allowed generic claim.

In view of the above noted withdrawal of the restriction requirement as to the linked species, applicant(s) are advised that if any claim(s) depending from or including all the limitations of the allowable generic linking claim(s) be presented in a continuation or divisional application, such claims may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 44 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

4. This application is in condition for allowance except for the following formal matter.

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Timothy B. Clise (reg. no. 40,957) on September 22, 2005.

The application has been amended as follows:

i. New claims 40 and 41 filed August 05, 2005 were incorrectly numbered and are **renumbered as claims 41 and 42**, respectively.

ii. **Claims 7, 8, 12, 13 are canceled** as being incorporated into their respective independent claims.

iii. In **claim 2**, delete "nickle" and insert "nickel".

iv. **Claims 1, 10, 24, 27 – 29, and 35** are amended and rewritten as follow.

1. A floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate;

wherein the control gate is separated from the floating gate by a low tunnel barrier integrate insulator having a thickness of less than 20 Angstroms;

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator; and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator.

10. A vertical memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate;

wherein the control gate is separated from the floating gate by a low tunnel barrier integrate insulator having a thickness of less than 20 Angstroms;

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator; and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator.

24. A method of forming a floating gate transistor, comprising:

forming a first source/drain region and a second source/drain region separated by a channel region in a substrate;

forming a floating ate opposing the channel region and separated therefrom by a gate oxide;

forming a control gate opposing the floating gate; and

forming a low tunnel barrier integrate insulator to separate the control gate from the floating gate, wherein forming the low tunnel barrier integrate insulator includes a tunnel barrier of less than 1.5 eV;

wherein forming the floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator; and

wherein forming the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator.

27. The method of claim 24, wherein forming the floating gate includes the metal layer being selected from the group consisting of platinum (Pt) and aluminum (Al).

28. The method of claim 24, wherein forming the control gate includes the metal layer being selected from the group consisting of platinum (Pt) and aluminum (Al).

29. A method for operating a DEAPROM memory cell, comprising:

writing to a floating gate of the DEAPROM memory cell using channel hot electron injection, wherein the DEAPROM memory cell includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate;

wherein the control gate is separated from the floating gate by a low tunnel barrier integrate insulator having a tunnel barrier of less than 1.5 eV,

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator, and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator; and

erasing charges from the floating gate by tunneling electrons off of the floating ate and onto the control gate by applying an electric field across the integrate insulator of 2.5×10^6 V/cm.

35. A method for operating an array of DEAPROM memory cells, comprising:

writing to one or more floating gates of a number of DEAPROM memory cells in the array of DEAPROM memory cells by tunneling electrons from a control gate through a low tunnel barrier integrate insulator having a tunnel barrier of less than 1.5 eV to a floating gate, wherein the array of DEAPROM memory cells includes:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried source lines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of DEAPROM

memory cells, wherein the number of control gates lines are separated from the floating gates by a low tunnel barrier integrate insulator;

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of DEAPROM cells,

wherein each the floating gates includes a polysilicon floating gate having a metal formed thereon in contact with the low tunnel barrier integrate insulator, and

wherein each the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator; and

erasing charges from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates through the low tunnel barrier integrate insulator.

Allowable Subject Matter

6. Claims 1 – 6, 9 – 11, and 14 – 42 are allowed.

7. The following is an examiner's statement of reasons for allowance:

The prior arts teach a floating gate/vertical floating gate transistor, comprising:

a first source/drain and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide; and

a control gate opposing the floating gate.

However, the prior arts fail to teach or reasonably suggest the floating gate transistor, further comprising in combination:

the control gate separated from the floating gate by an integrate insulator having a low tunnel barrier of less than 1.5 eV, or the integrate insulator having a thickness of less than 20 Angstroms,

further, the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator, and the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier integrate insulator.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
September 23, 2005

HUAN HOANG
PRIMARY EXAMINER